IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claims 1-47 (Canceled).

Claim 48 (New): A semiconductor device comprising:

a semiconductor substrate;

a memory cell having a channel and a gate insulating film formed on the semiconductor substrate, the gate insulating film comprising multiple layer films including a charge storage layer; and

shallow trench isolation regions formed in trenches provided in the semiconductor substrate, the memory cell being sandwiched between the shallow trench isolation regions;

wherein the shallow trench isolation regions include concave portions on upper ends thereof;

wherein the concave portions are formed above the charge storage layer; and

wherein a film thickness of the gate insulating film at a central portion of the channel and at portions contacting with the shallow trench isolation region are equal.

Claim 49 (New): The semiconductor device according to claim 48,

wherein the gate insulating film includes a first insulating film as the charge storage layer comprised of silicon and nitrogen as main constituent elements thereof and a second insulating film formed on the first insulating film, the second insulating film comprised of silicon and oxygen, and

wherein a film thickness of the second insulating film at a central portion of the channel and at portions contacting with the shallow trench isolation regions are equal.

Claim 50 (New): The semiconductor device according to claim 48,

wherein the gate insulating film includes a first insulating film as the charge storage layer comprised of silicon and nitrogen as main constituent elements thereof and a third insulating film formed between the first insulating film and the semiconductor substrate, the third insulating film comprised of silicon and oxygen, and

wherein a film thickness of the third insulating film at a central portion of the channel and at portions contacting with the shallow trench isolation regions are equal.

Claim 51 (New): The semiconductor device according to claim 48, further comprise a gate electrode on the gate insulating film,

wherein a width of the gate insulating film in a direction of the channel is equal to a width of the gate electrode in the direction of the channel.

Claim 52 (New): The semiconductor device according to claim 48, further comprising a gate electrode on the shallow trench isolation regions without interposition of the gate insulating film.

Claim 53 (New): The semiconductor device according to claim 52,

wherein the gate electrode contains impurities, and

wherein an impurity concentration of the gate electrode at a portion contacting with the gate insulating film is equal to an impurity concentration of the gate electrode at portions contacting with the shallow trench isolation regions.

Claim 54 (New): A semiconductor device comprising:

a semiconductor substrate;

a memory cell having a first channel and a first gate insulating film formed on the semiconductor substrate, the first gate insulating film comprising multiple layer films including a charge storage layer;

first shallow trench isolation regions formed in trenches provided in the semiconductor substrate, the memory cell being sandwiched between the first shallow trench isolation regions;

a transistor having a second channel and a second gate insulating film formed on the semiconductor substrate; and

second shallow trench isolation regions formed in trenches provided in the semiconductor substrate, the transistor being sandwiched between the second shallow trench isolation regions;

wherein the first shallow trench isolation regions have first concave portions on upper ends thereof;

wherein the second shallow trench isolation regions have second concave portions on upper ends thereof,

wherein the first concave portions are formed above the charge storage layer,

wherein a film thickness of the first gate insulating film at a central portion of the first channel and at portions contacting with the first shallow trench isolation regions are equal, and

wherein a film thickness of the second gate insulating film at a central portion of the second channel and at portions contacting with the second shallow trench isolation regions are equal.

Claim 55 (New): The semiconductor device according to claim 54,

wherein heights, from a surface of the semiconductor substrate, of upper surfaces of the first trench isolation regions are higher than heights, from the surface of the semiconductor substrate, of upper surfaces of the second trench isolation regions.

Claim 56 (New): The semiconductor device according to claim 54,

wherein the first gate insulating film includes a first insulating film as the charge storage layer comprised of silicon and nitrogen as main constituent elements thereof, a second insulating film formed on the first insulating film, the second insulating film comprised of silicon and oxygen, and a third insulating film formed between the first insulating film and the semiconductor substrate, the third insulating film comprised of silicon and oxygen, and

wherein a film thickness of the second insulating film at a central portion of the first channel and at portions contacting with the first shallow trench isolation regions are equal.

Claim 57 (New): The semiconductor device according to claim 54,

wherein the memory cell has a first gate electrode and the transistor has a second gate electrode, and

wherein the first gate electrode and the second gate electrode comprise polycrystalline silicon films, which are doped with impurities of conductivity types opposite to each other.